AMENDMENTS TO THE SPECIFICATION

Page 2, second full paragraph, please replace to read as follows:

The SONET standard, however, requires that the STS-1s that make up an STS-Nc occupy specific time slots. For example, Fig. ~~3~~ 2 illustrates 48 time slots occupied by 16 OC-3cs transmitted within an OC-48 frame. In particular, as seen in Fig. ~~3~~ 2, OC-3c #1 must occupy a "row" of time slots 1, 17 and 33, OC3-c #2 must occupy time slots 2, 18, and 34, and OC-3c #16, must occupy time slots 16, 32, and 48. In order to add a new OC-3c, one entire row shown in Fig. ~~3~~ 2, must be removed or reallocated.

Page 2, last paragraph, please replace to read as follows:

Fig. ~~4~~ 3 illustrates specific time slots occupied by four OC-12cs within an OC-48 frame. Specifically, OC-12c #1 must occupy time slots 1-4, 17-20, and 33-36, OC12-c #2 must occupy time slots 5-8, 21-24, and 37-40, and OC-12c #4 must occupy time slots 13-16, 29-32 and 45-48. Likewise, in order to add a new OC-12c, an entire row shown in Fig. ~~12~~ 3 must be removed or reallocated.

Page 3, first full paragraph, please replace to read as follows:

If time slots 1, 2 and 3 are dropped in the OC-48 frame shown in Fig. ~~3~~ 2, and populated with data for an OC-3c, however, they could not be switched by current SONET equipment because they are not transmitted in a sequence conforming to the concatenation protocol described above. Rather, a conventional SONET network element would need to be reconfigured to thereby rearrange the remaining time slots so that a new OC-48 frame is created which does conform to the standard concatenation sequence. If reconfiguration is not performed, the empty time slots cause bandwidth fragmentation.

Page 7, second full paragraph, please replace to read as follows:

The buses entering the switch, between stages, and leaving the switch are time-division multiplexed to carry an appropriate number of time slots. A switch element is capable of connecting any switch element input to any output, and of mapping any time slot on any input port to any time slot on any output port. Data entering the switch is typically converted from SONET frames into internal

switch frames including switch control information and several time slot groups containing data, as described for example in copending U.S. Patent Application No. 09/421,059 ~~Attorney Docket No. 288~~ entitled "A SWITCH MATRIX ARCHITECTURE AND TECHNIQUES FOR IMPLEMENTING RAPID HITLESS SWITCHOVER", filed on October 19, 1999, which is incorporated by reference herein.

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